IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	10/674,085
Applicant	:	Elias Fallon et al.
Filed	:	September 29, 2003
Title	:	**METHOD FOR GENERATING CONSTRAINED COMPONENT PLACEMENT FOR INTEGRATED CIRCUITS AND PACKAGES**
Group Art Unit	:	Not Yet Assigned
Examiner	:	Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to the requirements of 37 C.F.R. §§1.56, 1.97 and 1.98, Applicants submit this Information Disclosure Statement together with completed Form(s) PTO/SB/08A and a copy of each reference listed thereon.

Pursuant to the Notice regarding Information Disclosure Statements appearing in 1276 OG 55, dated August 5, 2003, no copy of each United States Patent or Patent Application Publication listed on the Form(s) PTO/SB/08A is included herewith.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on February 2, 2004.

Deborah L. Medves
(Name of Person Mailing Papers)

Deborah L. Medves 02/02/04
Signature Date

No fee is believed to be due for the filing of this Information Disclosure Statement as it is being submitted before a first Office Action on the Merits. Nevertheless, the Commissioner of Patents and Trademarks is hereby authorized to charge any additional fees which may be required to Deposit Account No. 23-0650. One (1) original and two (2) copies of this Information Disclosure Statement are enclosed.

Respectfully submitted,

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Sheet 1 of 3

Complete if Known	
Application Number	10/674,085
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First Named Inventor	Elias Fallon et al.
Group Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	2879-030564

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2]	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	6,161,078		Ganley	12/12/2000	
	2	6,282,694		Cheng et al.	08/28/2001	
	3	6,550,046	B1	Balasa et al.	04/15/2003	

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, cite and/or country where published.	T[2]
	4	FLORIN BALASA and KOEN LAMPAERT, "Module Placement For Analog Layout Using The Sequence-Pair Representation", Proc. ACM/IEEE Design Automation, pp. 274-279, (June 1999).	
	5	FLORIN BALASA and KOEN LAMPAERT, "Symmetry Within The Sequence-Pair Representation In The Context Of Placement For Analog Design", IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 19, No. 7, pp. 721-731 (July 2000).	
	6	FLORIN BALASA, "Device-Level Placement For Analog Layout: An Opportunity For Non-Slicing Topological Representations", Proc. Asia-Pacific DAC (ASPDAC), pp. 281-286, (2001).	
	7	ERIC FELT, ENRICO MALAVASI, EDOARDO CHARBON, ROBERTO TOTARO and ALBERTO SANGIOVANNI-VINCENTELLI, "Performance-Driven Compaction For Analog Integrated Circuits", IEEE 1993 Custom Integrated Circuits Conference, pp. 17.3.1-17.3.5, (1993).	
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	10	PEI-NING GUO, CHUNG-KUAN CHENG and TAKESHI YOSHIMURA, "An O-Tree Representation Of Non-Slicing Floorplan And Its Applications", Proc. ACM/IEEE Design Automation Conference, pp. 268-273, (June 1999).	
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Examiner Signature		Date Considered	

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	14	MARGHERITA PILLAN and DONATELLA SCIUTO, "Constraint Generation And Placement For Automatic Layout Design Of Analog Integrated Circuits", pp. 355-358.	
	15	YINGXIN PANG, FLORIN BALASA, KOEN LAMPAERT and CHUNG-KUAN CHENG, "Block Placement Symmetry Constraints Based On The O-Tree Non-Slicing Representation", Proc. ACM/IEEE Design Automation Conference, pp. 464-467, (June 2000).	
	16	JUAN A. PRIETO, JOSE M. QUINTANA, ADORACION RUEDA and JOSE L. HUERTAS, "An Algorithm For The Place-And-Route Problem In The Layout Of Analog Circuits", Pro. IEEE ISCAS, pp. 491-494 (1994).	
	17	D. F. WONG and C. L. LIU, "A New Algorithm For Floorplan Design", Proceedings Of The 23rd ACM/IEEE Design Automation Conference, pp. 101-107, (July 1986).	
	18	JOHN M. COHN, DAVID J. GARROD, ROB A. RUTENBAR and L. RICHARD CARLEY, "KOAN/ANAGRAM II: New Tools For Device-Level Analog Placement And Routing," IEEE Journal Of Solid-State Circuits, Vol. 26, No. 3, pp. 330-342, (March 1991).	
	19	D. W. JEPSEN and C.D. GELLAT JR., "Macro Placement By Monte Carlo Annealing", Proc. IEEE International Conference On Computer Design, pp. 495-498, (November 1984).	
	20	ENRICO MALAVASI, EDOARDO CHARBON, GANI JUSUF, ROBERTO TOTARO and ALBERTO SANGIOVANNI-VINCENTELLI, "Virtual Symmetry Axes For The Layout Of Analog IC's", Proc. 2nd ICVC, pp. 1-10, (October 1991).	
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	22	HIROSHI MURATA, KUNIHIRO FUJIYOSHI, SHIGETOSHI NAKATAKE and YOJI KAJITANI, "VLSI Module Placement Based On Rectangle-Packing By The Sequence-Pair", IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 15, No. 12, pp. 1518-1524, (December 1996).	
	23	SUJOY MITRA, SUDIP K. NAG, ROB A. RUTENBAR and L. RICHARD CARLEY, "System-Level Routing Of Mixed-Signal ASICS In WREN", Proc. ACM/IEEE International Conference On CAD, pp. 394-399, (November 1992).	

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	24	R. OKUDA, T. SATO, H. ONODERA and K. TAMARU, "An Efficient Algorithm For Layout Compaction Problem With Symmetry Constraints", In Proc. IBBB ICCAD, pp. 148-151, (November 1989).	

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